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Application Note: Virtex-II, Virtex-II Pro, and Spartan-3 Families



XAPP774 (v1.2) February 23, 2006

Connecting Xilinx FPGAs to Texas Instruments ADS527x Series ADCs

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Summary

This application note describes how to connect a high-speed Texas Instruments (TI) ADS5273 serial-to-digital converter (ADC) with serialized LVDS output to a Virtex™-II or Virtex-4 Pro FPGA. Lower speed ADC devices from this family can be connected to Spartan™-3 FPGAs.

Introduction

Texas Instruments has an 8-channel, 12-bit ADC family with synchronous LVDS outputs. The performance rates of these ADCs range from 40 MSPS to 70 MSPS. This family fits nicely with the LVDS IOs of the Virtex-II, Virtex-II Pro, and Spartan-3 devices.

To highlight the performance of the ADCs in the FPGA, the reference design described in the Application note uses an ADC device which is a high-speed sampling ADC. The ADS5273 integrates an XC7V250-FT256 device or the Texas Instruments demo board and to an XC2VP30-6TF366 device on the Xilinx demo boards.

ADS527x ADCs

The ADS527x components are 8-channel, 12-bit analog-to-digital converters with serialized LVDS interfaces and sample rates from 40 MSPS to 70 MSPS. This section summarizes their features and applications. For complete information, refer to the TI website at:

<http://focus.ti.com/iusl/connote/connoteinfo.cfm?connoteid=13&connoteid=2&connoteid=3&connoteid=4&connoteid=5>

Features

- The key features of the ADS527x family are:
 - Maximum sample rate of 40 MSPS (ADS5279), 50 MSPS (ADS5271), 65 MSPS (ADS5272), and 70 MSPS (ADS5273).
 - 12-bit resolution
 - No missing codes
 - Power dissipation of 1.1W
 - CMOS technology
 - Simultaneous sample and hold
 - 70.3 dB signal-to-noise ratio (SNR) on a 10 MHz interface
 - Serialized LVDS outputs meet or exceed the requirements of the ANSI TIA/EIA-644-A standard
 - Internal and external references
 - 3.3V digital/analog supply
 - TQFP-60 PowerPAD package

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Table 2-3: Available Integrated Blocks for PCI Express

Device Selection		Integrated Block for PCI Express Location			
Device	Package	X0Y0	X0Y1	X0Y2	X0Y3
XC7VX330T	FFG1157 FFG1761	Yes	Yes		
XC7VX415T	FFG1157 FFG1158 FFG1927 FFV1157 FFV1761	Yes	Yes		
XC7VX550T	FFG1158 FFV1157 FFV1158 FFV1927 FFG1927		Yes	Yes	
XC7VX690T	FFG1157 FFG1158 FFG1930 FFG1761 FFG1926 FFG1927		Yes	Yes	
XC7VX980T	FFG1926 FFG1928 FFG1930	Yes	Yes	Yes	
XC7VX1140T	FLG1926 FLG1928 FLG1930	Yes	Yes	Yes	Yes
XC7VH580T	FLG1155 FLG1931 HCG115	Yes			
XC7VH870T	FLG1932 HCG1931	Yes	Yes	Yes	
XC7VX330T	RF1157 HCG1932 RF1761	Yes	Yes		

Gen3 Integrated Block for PCIe v4.3

PG023 October 4, 2017

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12

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User Guide

Revision A (0.4)

2008-03-04

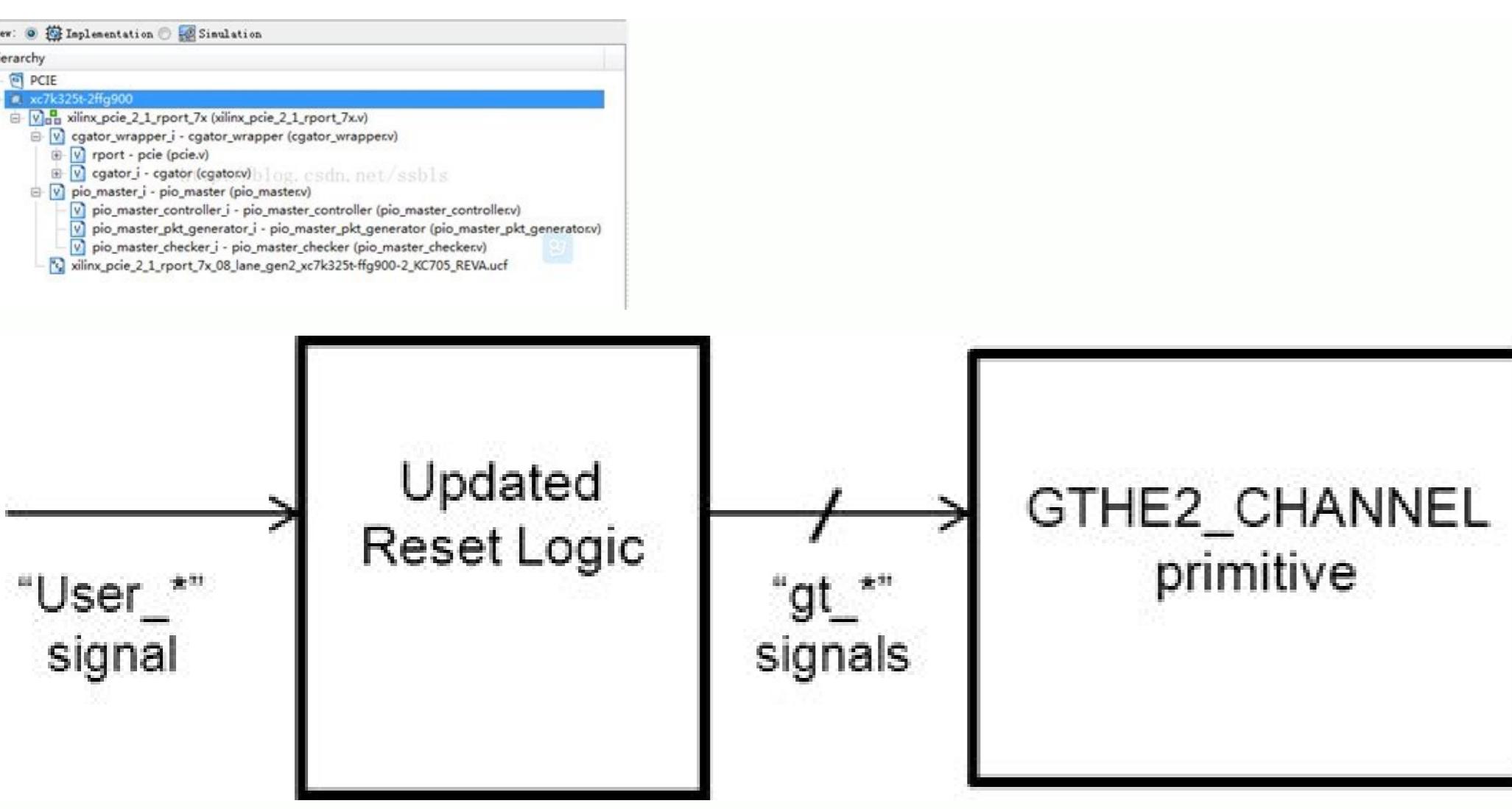
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